What is claimed is:

[c1] 1.A communications processor implemented on a chip, comprising:
a network processor including means for processing a plurality of protocols including ATM, frame relay, Ethernet, and IP, said means being programmable using a set of library commands to process additional protocols;
a protocol processor for controlling the network processor;
wherein the protocol processor performs control plane processing and the network processor performs data plane processing; and
wherein the network processor and the protocol processor are ring members on at least one ring network, and further comprising a plurality of other ring members on the at least one ring network.

[c2] 2.The communications processor of claim 1, wherein the network processor includes a plurality of compounds that share a single ring interface to the ring network.

[c3] 3.The communications processor of claim 1, wherein the communications processor is PHY neutral.

[c4] 4.The communications processor of claim 1, wherein the at least one ring network comprises multiple ring networks including a protocol processor ring network and a network processor ring network.

[c5] 5.The communications processor of claim 4, where the network processor ring network includes a first network processor for transmitting packets and a second network processor for receiving packets.

[c6] 6.The communication processor of claim 1, wherein the network processor includes ultrafast task switching using active registers for current tasks and shadow registers for preloading next tasks.

[c7] 7.The communications processor of claim 1, further comprising multiple DMA controllers for access to external memories.

[c8] 8.The communications processor of claim 1, wherein the protocol processor is adapted to perform the following: signaling protocols; protocol management;

exception handling; and system configuration and control.

[c9] 9.The communications processor of claim 1, wherein the network processor is adapted to perform the following: per-packet processing; packet forwarding; packet classification; quality-of-service handling; and packet reformatting.

[c10] 10.The communications processor of claim 1, wherein the control path protocol support is provided by the protocol processor and the data path protocol support is provided by the network processor.

[c11] 11.The communications processor of claim 1, wherein the network processor performs zero overhead task switching.

[c12] 12.The communications processor of claim 1, wherein the network processor includes compound modules operating as parallel engines.

[c13] 13.The communications processor of claim 1, wherein the communications processor is implemented to provide an enterprise integrated access device (EIAD).

[c14] 14.The communications processor of claim 1, wherein the communications processor is implemented to provide a multi-tenant unit (MTU) or remote terminal unit (RTU).

[c15] 15.The communications processor of claim 1, wherein the communications processor is implemented to provide a media gateway.

[c16] 16.The communications processor of claim 1, wherein the communications processor is implemented to provide a voice gateway.